<<嵌入式微控制器与处理器设计>>

图书基本信息

书名：<<嵌入式微控制器与处理器设计>>

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前言

Microcontrollers have become ubiquitous elements of everyday life. Most of the electronic prod ucts we use in daily lite have a microconlroller rocked inside. They are used in household appli-ances, automobiles, copiers, cell phones, and even used to control powerful locomotives. Where electricity is used, you will find a microcontroller! There are many technical books on the subject of microcontrollers. Why develop a new book'? All the popular microcontroller chips and architectures have "howm" books in print. The locus of this text is a broader introduction to the student of microcontroller processor technology,both in singlechip and intellectual property form. Many electronic engineering students are required to take a course in embedded system de-sign with microcontrollers. Devices such as the Intel 8051, ZILOG Z8, or Microchip PlC are most often the microcontroller of choice because of their widespread popularity. Als(), they have extensive, inexpensive tools available to provide design support. A wider variety of choices for an embedded microcontroller-based design face the engineer today, not only the popular single-chip devices, but also intellectual property cores for ASIC system-on-a-chip (SEC) design. Although the computer world has solidified around Intel-based archi-tectures, the microcontroller world continues to evolve with innovative new designs. This book is organized into three major sections: an introduction Itl microcontroller ar chitectures, single-chip microcontrollers, and embedded IP cores. Each chapter within the section begins with learning objectives. Questions are provided at the end of the section to monitor progress. Not only are specific chips and cores covered, but also this book introduces the student to the concepts of microcontroller architectures: for instance, how the concept of the computing de-vices evolved, and why different types of devices are used in design. Single-chip microcontrollers as referenced in this book are typical commercial high-volume classical designs. Certainly, myriad parts are also available, particularly from "fab-less" design houses. Microcontroller cores are in reference to established system-on-achip intellectual property cores and marketed as such. In architectural discussions in this book, the term "processor" incorporates both the "processor" element of "singlechip microcontrollers"and "IP cores." This book is intended to provide the reader with an introduction to single-chip and embed-ded microcontroller processor design. The difference between architectures of the CISC- and RISC-based processors is discussed. Single-chip microcontroller design flows and embedded processor design flows are discussed. The 16-bit Freescale MC9SI2X family of singlechip microcontrollers is covered in detail. The RISC-based P1ClgF4520 and the ZILOG Z8 Encore! 8-bit microcontrollers are also discussed. The peripherals that are available with various members of the families are explained. The concept of instruction set architecture (ISA) is introduced to develop an understanding of the commonality of the CISC and RISC processor families, respectively. This is expanded to the design of SoC embedded controllers-based core IP using the ISAs of ARM and MIPS. The ARM10TDMI and MIPS32 4KETM IP cores are presented in some detail. Configurable processor technology is increasingly important, particularly in the design of higher performing consumer products. It allows customization of the core processor, which can have both performance and power impact on the SoC embedded design. The Tensillica Xtensa LX2 Series configurable processor is covered. A discussion of derivative RISC application-specific processors is presented. An overview of a digital signal processors (DSP), including the Texas Instruments' TMS320C55 and Analog Devices' ADSP-BR533 Blackfin is given. The methodology of the engineering design flow is also covered. Different tools available to the engineer for the design process are discussed. An example of using an integrated design environment (IDE) for single-chip micro-controller is presented. Software programming for microcontroller design can be as simple as a program for controlling lawn sprinklers to a complex RTOS for robots. Programming techniques from simple polling loops to multilevel interrupt driven systems are discussed. Many single-chip microcon-trollers include functional blocks for serial I/O. They are primarily used to communicate data.The UART, 12C, I2S, CAN/LIN SPI, and USB peripheral functions are discussed. System-on-a-chip design requires a close relationship with the semiconductor foundry. As a fabless design technology, SoCs need specialized engineering techniques to integrate the functions needed for the chip. Combining IP functional blocks available from the foundry with those from independent companies to achieve a working chip is a complex process. This book is intended as an introductory understanding of microcontrollers in

singlechip and embedded forms. The concept of ISA is developed with the methodology for product design.System-on-a-chip design is introduced through the use of intellectual property. Microcontroller design, at any level of abstraction, is based on a balancing of available technologies. The primary three technologies this book will locus on are processor, memory, and software: processor technology as it is defined in terms of semiconductor fabrication capability;memory technology as it is implemented in a hierarchical storage structure; and software tech-nology as it is implemented in the form of assembler and optimizing compilers. Within the scope of this book, generalizations are taken as they relate to characteristics of microcontroller-based design. In general, CISC-based processors have more complex instructions than RISC-based processors. In general, RISC registers sets are orthogonal when compared to CISC. In general, optimizing C compilers are more efficient for RISC than CISC. RISC and CiSC are considered in their global context of instruction set architecture (ISA). New innovations in architecture, such as VLIW and EPIC, are mentioned for compari-son. The focus of this book is on microcontroller technology, which is predominately RISC- or CISC-based. This will provide the basic knowledge needed for the student to understand other derivative ISAs. Microcontrollers have, at their heart, a microprocessor. In this book, the term processor is used in a broad sense. Whether implemented as core IP in an SoC, or in traditional single-chip form, the basic concept of the processor is the same. MIPS32 4KETM IP can be incorporated as single chips from NEC or an SoC in a CISCO router. They are implemented differently but are the same architecturally. This book is intended as an introduction to the topic of microcontroller technology for college engineering students. It is not a hardware reference manual. It is not intended al a series Of application notes. The concepts presented are in general form. This will allow a broad group of engineering students to understand the basic concepts and apply them to realworld situations. .An online instructor's manual is available for instructors using this text for a course. To access supplementary materials online, instructors need to request an instructor access code. Go to www. pearsonhighered.com/irc, where you can register for an instructor access code.Within 48 hours after registering, you will receive a confirming e-mail, including an instructor access code. Once you have received your code, go to the site and log on for full instructions on downloading the materials you wish to use. The author thanks the following reviewers of the manuscript: C. Richard G. Helps,Brigham Young University; James Streib, Illinois College; Chao-Ying Wang, DeVry Univer-sity-Columbus; and Richard Warren, Vermont Technical College. Greg Osborn

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内容概要

本书全面讲述了嵌入式微控制器的基础知识，重点在于让学生理解微控制器背后的基本概念，而不在于教授学生为某个具体器件编写软件。
全书内容覆盖如下主要概念：数字信号处理、模糊逻辑和模数转换，以便学生更好地理解现实世界中的设计理念。
本书强调微控制器处理器架构和技术的特点，使其更适合用作高校电子电气工程、计算机以及工程技术类相关专业的教材，还可用作专业嵌入式微控制器设计人员的参考书。

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书籍目录

章节摘录

插图：sequencer controls the flow of instruction execution.including instruction alignment and decoding.The sequencer supports conditional jumps and subroutine calls， as well as zerooverhead looping.A loop buffer stores instructions locally,eliminating instruction memory accesses for tightly looped code.Two data address generators(DAGs)provide addresses for simultaneous dual operand fetches from memory.The DAGs share a register file containing four sets of 32-bit index,mod-ify,length， and base registers.Eight additional 32-bit registers provide pointers for general indexing of variables and stack locations.Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure.Level 1 (Ll)memories are those that typically operate at the full processor speed with little or no latency.Level 2(L2)memories are other memories.on-chip or off-chip.that may take multiple processor cycles to access， At the L1 1evel。
the instruction memory holds instructions only.The two data memories hold data， and a dedicated scratch pad data memory stores stack and local variable information.At the L2 level.there is a single unified memory space.holding both instructions and data.In addition.the L1 instruction memory and L1 data memories may be configured as either static RAMs(SRAMs)or caches.The memory management unit(MMU)provides memory protection for individual tasks that mav be operating on the core and may protect system registers from unintended access.The architecture provides three modes of operation：user mode， supervisor mode， and emulation mode.User mode has restricted access to certain system resources， thus providing a protected software environment， whereas supervisor mode has unrestricted access to the system and core resources.The Blackfin processor instruction set has been optimized so that 16-bit op codes represent the most frequently used instructions ， resulting in excellent compiled code density.Complex DSP instructions are encoded into 32-bit op codes.representing fully featured multifunction instructions.Blackfin processors support a limited multiple issue capability， where a 32-bit instruction can be issued in parallel with two 16-bit instructions.allowing the programmer to usemany of the core resources in a single instruction cycle.The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability.The architecture has been optimized for use in conjunction with the C／C++compiler,resulting in fast and efficient software implementations.15.213.1 Instruction Pipeline The program sequencer determines the next instruction address by examining both the current instruction being executed and the current state of the processor.If no conditions require otherwise， the processor executes instructions from memory in sequential order by incrementing the lookahead address.The processor has a ten-tage instruction pipeline with the stages 1isted in Figure 15.25.15.2.Instruction Pipeline Flow Figure 15.26 shows a diagram ofthe processor pipeline.The instruction fetch and branch logic generates 32-bit fetch addresses for the instruction memory unit.The instruction alignment unit returns instructions and their width information at the end of the IF3 stage.For each instruction type(16， 32， or 64 bits)， the instruction alignment unit ensures that the alignment buffers have enough valid instructions to be able to provide an instruction every cycle.Because the instructions can be 1 6.32.or 64 bits wide.the instruction alignment unit may not need to fetch an instruction from the cache every cycle.For a series of 16.bit instructions.the instruction alignment unit gets an instruction from the instruction memory unit once in four cycles.The alignment logic requests the next instructtion address based on the status of the alignment buffers.The sequencer responds by generating the next fetch address in the next cycle.provided there is no change of flow.

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