<<System Verilog数字系统设 >

图书基本信息

书名：<<System Verilog数字系统设计>>

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作者：马克

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内容概要

SystemVerilog是21世纪电子设计师必须掌握的最重要的语言之一，因为它是设计和验证复杂电子系统核心芯片的重要手段。
由马克编写的这本《System
Verilog
数字系统设计(影印版)》是用SystemVerilog语言设计并验证数字系统的基本概念和具体方法。
在介绍基本语法的基础上，阐述了如何用
SystemVerilog构成数字电路、组件和系统，以及应该如何使用SystemVerilog搭建测试平台，并对设计进行验证。

《System Verilog数字系统设计(影印版)》既适合作电子、自动化和计算机专业本科生和研究生的教科书，也适合已经掌握
Verilog和VHDL硬件描述语言的工程师使用。

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版权页： 插图： 3.5 Logic Values In the preceding description,we mentioned logic values and referred briefly to a high impedance state.SystemVerilog allows wires to take four possible values: 0,1,x (unknown),and z (high impedance).In general,logic gates are designed to generate 0 or 1 at the outputs,x usually indicates some kind of anomalous situation-perhaps an unimtialized flip-flop or a wire that is being driven to two different values by two gates simultaneously. The high-impedance state,z,is used to model the output of three-state buffers.The purpose of three-state buffers is to allow the outputs of gates to be connected together to form buses,for example.The x state is normally generated when different outputs from two gates are connected together.We would expect,however,that a 1 and a z (or a 0 and a z) driving the same wire would resolve to a 1 (or a 0).Clearly,therefore,not all logic values are equal. The unknown and high-impedance states can be written as lower case ("x" and "z") or upper case ("X" and "Z") characters.The question mark ("?") can be used as an alternative to the high-impedance state. 3.6 Continuous Assignments The two-input AND gate at the beginning of the chapter was written using a continuous assignment.In general,continuous assignments are used to assign values to nets.In later chapters,we will see that alwaya comb and always ff procedural blocks are more useful for describing synthesizable hardware.Continuous assignments are,on the other hand,the most convenient way to describe three-state buffers and to model delays in combinational logic.Three-state buffers will be discussed in more detail in the next chapter.This is an appropriate point,however,to discuss SystemVerilog operators.

编辑推荐

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