

<<功率半导体器件基础>>

图书基本信息

书名：<<功率半导体器件基础>>

13位ISBN编号：9787030343406

10位ISBN编号：7030343409

出版时间：2012-6

出版时间：科学出版社

作者：巴利伽

页数：1065

字数：1378000

版权说明：本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问：<http://www.tushu007.com>

## <<功率半导体器件基础>>

### 内容概要

《功率半导体器件基础（英文版）》作者是功率半导体器件领域的著名专家，IGBT器件发明人之一。  
《功率半导体器件基础（英文版）》结合作者多年的实践经验，深入讨论了半导体功率器件的物理模型、工作原理、设计原则和应用特性，不仅详细介绍了硅基器件，还讨论了碳化硅器件的特性与设计要求。

主要内容包括材料特性与输运物理、击穿电压、肖特基整流器、P-i-N整流器、功率MOSFET器件、双极型晶体管、晶闸管、IGBT器件等。

《功率半导体器件基础（英文版）》可作为微电子、电力电子等相关领域科研人员、工程技术人员的参考书，也可作为相关专业高年级本科生、研究生的教材。

<<功率半导体器件基础>>

作者简介

无

## &lt;&lt;功率半导体器件基础&gt;&gt;

## 书籍目录

Preface  
 Chapter 1 Introduction  
 1.1 Ideal and Typical Power Switching Waveforms  
 1.2 Ideal and Typical Power Device Characteristics  
 1.3 Unipolar Power Devices  
 1.4 Bipolar Power Devices  
 1.5 MOS-Bipolar Power Devices  
 1.6 Ideal Drift Region for Unipolar Power Devices  
 1.7 Charge-Coupled Structures: Ideal Specific On-Resistance  
 1.8 Summary  
 Problems  
 References  
 Chapter 2 Material Properties and Transport Physics  
 2.1 Fundamental Properties  
 2.1.1 Intrinsic Carrier Concentration  
 2.1.2 Bandgap Narrowing  
 2.1.3 Built-in Potential  
 2.1.4 Zero-Bias Depletion Width  
 2.1.5 Impact Ionization Coefficients  
 2.1.6 Carrier Mobility  
 2.2 Resistivity  
 2.2.1 Intrinsic Resistivity  
 2.2.2 Extrinsic Resistivity  
 2.2.3 Neutron Transmutation Doping  
 2.3 Recombination Lifetime  
 2.3.1 Shockley-Read-Hall Recombination  
 2.3.2 Low-Level Lifetime  
 2.3.3 Space-Charge Generation Lifetime  
 2.3.4 Recombination Level Optimization  
 2.3.5 Lifetime Control  
 2.3.6 Auger Recombination  
 2.4 Ohmic Contacts  
 2.5 Summary  
 Problems  
 References  
 Chapter 3 Breakdown Voltage  
 3.1 Avalanche Breakdown  
 3.1.1 Power Law Approximations for the Impact Ionization Coefficients  
 3.1.2 Multiplication Coefficient  
 3.2 Abrupt One-Dimensional Diode  
 3.3 Ideal Specific On-Resistance  
 3.4 Abrupt Punch-Through Diode  
 3.5 Linearly Graded Junction Diode  
 3.6 Edge Terminations  
 3.6.1 Planar Junction Termination  
 3.6.2 Planar Junction with Floating Field Ring  
 3.6.3 Planar Junction with Multiple Floating Field Rings  
 3.6.4 Planar Junction with Field Plate  
 3.6.5 Planar Junction with Field Plates and Field Rings  
 3.6.6 Bevel Edge Terminations  
 3.6.7 Etch Terminations  
 3.6.8 Junction Termination Extension  
 3.7 Open-Base Transistor Breakdown  
 3.7.1 Composite Bevel Termination  
 3.7.2 Double-Positive Bevel Termination  
 3.8 Surface Passivation  
 3.9 Summary  
 Problems  
 References  
 Chapter 4 Schottky Rectifiers  
 4.1 Power Schottky Rectifier Structure  
 4.2 Metal-Semiconductor Contact  
 4.3 Forward Conduction  
 4.4 Reverse Blocking  
 4.4.1 Leakage Current  
 4.4.2 Schottky Barrier Lowering  
 4.4.3 Prebreakdown Avalanche Multiplication  
 4.4.4 Silicon Carbide Rectifiers  
 4.5 Device Capacitance  
 4.6 Thermal Considerations  
 4.7 Fundamental Tradeoff Analysis  
 4.8 Device Technology  
 4.9 Barrier Height Adjustment  
 4.10 Edge Terminations  
 4.11 Summary  
 Problems  
 References  
 Chapter 5 P-i-N Rectifiers  
 5.1 One-Dimensional Structure  
 5.1.1 Recombination Current  
 5.1.2 Low-Level Injection Current  
 5.1.3 High-Level Injection Current  
 5.1.4 Injection into the End Regions  
 5.1.5 Carrier-Carrier Scattering Effect  
 5.1.6 Auger Recombination Effect  
 5.1.7 Forward Conduction Characteristics  
 5.2 Silicon Carbide P-i-N Rectifiers  
 5.3 Reverse Blocking  
 5.4 Switching Performance  
 5.4.1 Forward Recovery  
 5.4.2 Reverse Recovery  
 5.5 P-i-N Rectifier Structure with Buffer Layer  
 5.6 Nonpunch-Through P-i-N Rectifier Structure  
 5.7 P-i-N Rectifier Tradeoff Curves  
 5.8 Summary  
 Problems  
 References  
 Chapter 6 Power MOSFETs  
 6.1 Ideal Specific On-Resistance  
 6.2 Device Cell Structure and Operation  
 6.2.1 The V-MOSFET Structure  
 6.2.2 The VD-MOSFET Structure  
 6.2.3 The U-MOSFET Structure  
 6.3 Basic Device Characteristics  
 6.4 Blocking Voltage  
 6.4.1 Impact of Edge Termination  
 6.4.2 Impact of Graded Doping Profile  
 6.4.3 Impact of Parasitic Bipolar Transistor  
 6.4.4 Impact of Cell Pitch  
 6.4.5 Impact of Gate Shape  
 6.4.6 Impact of Cell Surface Topology  
 6.5 Forward Conduction Characteristics  
 6.5.1 MOS Interface Physics  
 6.5.2 MOS Surface Charge Analysis  
 6.5.3 Maximum Depletion Width  
 6.5.4 Threshold Voltage  
 6.5.5 Channel Resistance  
 6.6 Power VD-MOSFET On-Resistance  
 6.6.1 Source Contact Resistance  
 6.6.2 Source Region Resistance  
 6.6.3 Channel Resistance  
 6.6.4 Accumulation Resistance  
 6.6.5 JFET Resistance  
 6.6.6 Drift Region Resistance  
 6.6.7 N+ Substrate Resistance  
 6.6.8 Drain Contact Resistance  
 6.6.9 Total On-Resistance  
 6.7 Power VD-MOSFET Cell Optimization  
 6.7.1 Optimization of Gate Electrode Width  
 6.7.2 Impact of Breakdown Voltage  
 6.7.3 Impact of Design Rules  
 6.7.4 Impact of Cell Topology  
 6.8 Power U-MOSFET On-Resistance  
 6.8.1 Source Contact Resistance  
 6.8.2 Source Region Resistance  
 6.8.3 Channel Resistance  
 6.8.4 Accumulation Resistance  
 6.8.5 Drift Region Resistance  
 6.8.6 N+ Substrate Resistance  
 6.8.7 Drain Contact Resistance  
 6.8.8 Total On-Resistance  
 6.9 Power U-MOSFET Cell Optimization  
 6.9.1 Orthogonal P-Base Contact Structure  
 6.9.2 Impact of Breakdown Voltage  
 6.9.3 Ruggedness Improvement  
 6.10 Square-Law Transfer Characteristics  
 6.11 Superlinear Transfer Characteristics  
 6.12 Output Characteristics  
 6.13 Device Capacitances  
 6.13.1 Basic MOS Capacitance  
 6.13.2 Power VD-MOSFET Structure Capacitances  
 6.13.3 Power U-MOSFET Structure Capacitances  
 6.13.4 Equivalent Circuit  
 6.14 Gate Charge  
 6.14.1 Charge Extraction  
 6.14.2 Voltage and Current Dependence  
 6.14.3 VD-MOSFET vs. U-MOSFET Structure  
 6.14.4 Impact of

## &lt;&lt;功率半导体器件基础&gt;&gt;

VD-MOSFET and U-MOSFET Cell Pitch6.15 Optimization for High Frequency Operation6.15.1 Input Switching Power Loss6.15.2 Output Switching Power Loss6.15.3 Gate Propagation Delay6.16 Switching Characteristics6.16.1 Turn-On Transient6.16.2 Turn-Off Transient6.16.3 Switching Power Losses6.16.4  $[dV/dt]$  Capability6.17 Safe Operating Area6.17.1 Bipolar Second Breakdown6.17.2 MOS Second Breakdown6.18 Integral Body Diode6.18.1 Reverse Recovery Enhancement6.18.2 Impact of Parasitic Bipolar Transistor6.19 High-Temperature Characteristics6.19.1 Threshold Voltage6.19.2 On-Resistance6.19.3 Saturation Transconductance6.20 Complementary Devices6.20.1 The p-Channel Structure6.20.2 On-Resistance6.20.3 Deep-Trench Structure6.21 Silicon Power MOSFET Process Technology6.21.1 Planar VD-MOSFET Process6.21.2 Trench U-MOSFET Process6.22 Silicon Carbide Devices6.22.1 The Baliga-Pair Configuration6.22.2 Planar Power MOSFET Structure6.22.3 Shielded Planar Power MOSFET Structures6.22.4 Shielded Trench-Gate Power MOSFET Structure6.23 SummaryProblemsReferencesChapter 7 Bipolar Junction Transistors7.1 Power Bipolar Junction Transistor Structure7.2 Basic Operating Principles7.3 Static Blocking Characteristics7.3.1 Open-Emitter Breakdown Voltage7.3.2 Open-Base Breakdown Voltage7.3.3 Shorted Base-Emitter Operation7.4 Current Gain7.4.1 Emitter Injection Efficiency7.4.2 Emitter Injection Efficiency with Recombination in the Depletion Region7.4.3 Emitter Injection Efficiency with High-Level Injection in the Base7.4.4 Base Transport Factor7.4.5 Base Widening at High Collector Current Density7.5 Emitter Current Crowding7.5.1 Low-Level Injection in the Base7.5.2 High-Level Injection in the Base7.5.3 Emitter Geometry7.6 Output Characteristics7.7 On-State Characteristics7.7.1 Saturation Region7.7.2 Quasisaturation Region7.8 Switching Characteristics7.8.1 Turn-On Transition7.8.2 Turn-Off Transition7.9 Safe Operating Area7.9.1 Forward-Biased Second Breakdown7.9.2 Reverse-Biased Second Breakdown7.9.3 Boundary for Safe Operating Area7.10 Darlington Configuration7.11 SummaryProblemsReferencesChapter 8 Thyristors8.1 Power Thyristor Structure and Operation8.2 Blocking Characteristics8.2.1 Reverse-Blocking Capability8.2.2 Forward-Blocking Capability8.2.3 Cathode Shorting8.2.4 Cathode Shorting Geometry8.3 On-State Characteristics8.3.1 On-State Operation8.3.2 Gate-Triggering Current8.3.3 Holding Current8.4 Switching Characteristics8.4.1 Turn-On Time8.4.2 Gate Design8.4.3 Amplifying Gate Design8.4.4  $[dV/dt]$  Capability8.4.5 Turn-Off Process8.5 Light-Activated Thyristors8.5.1  $[dI/dt]$  Capability8.5.2 Gate Region Design8.5.3 Optically Generated Current Density8.5.4 Amplifying Gate Design8.6 Self-Protected Thyristors8.6.1 Forward Breakdown Protection8.6.2  $[dV/dt]$  Turn-On Protection8.7 The Gate Turn-Off Thyristor Structure8.7.1 Basic Structure and Operation8.7.2 One-Dimensional Turn-Off Criterion8.7.3 One-Dimensional Storage Time Analysis8.7.4 Two-Dimensional Storage Time Model8.7.5 One-Dimensional Voltage Rise Time Model8.7.6 One-Dimensional Current Fall Time Model8.7.7 Switching Energy Loss8.7.8 Maximum Turn-Off Current8.7.9 Cell Design and Layout8.8 The Triac Structure8.8.1 Basic Structure and Operation8.8.2 Gate-Triggering Mode 18.8.3 Gate-Triggering Mode 28.8.4  $[dV/dt]$  Capability8.9 SummaryProblemsReferencesChapter 9 Insulated Gate Bipolar Transistors9.1 Basic Device Structures9.2 Device Operation and Output Characteristics9.3 Device Equivalent Circuit9.4 Blocking Characteristics9.4.1 Symmetric Structure Forward-Blocking Capability9.4.2 Symmetric Structure Reverse-Blocking Capability9.4.3 Symmetric Structure Leakage Current9.4.4 Asymmetric Structure Forward-Blocking Capability9.4.5 Asymmetric Structure Reverse-Blocking Capability9.4.6 Asymmetric Structure Leakage Current9.5 On-State Characteristics9.5.1 On-State Model9.5.2 On-State Carrier Distribution:Symmetric Structure9.5.3 On-State Voltage Drop:Symmetric Structure9.5.4 On-State Carrier Distribution:Asymmetric Structure9.5.5 On-State Voltage Drop:Asymmetric Structure9.5.6 On-State Carrier Distribution:Transparent Emitter Structure9.5.7 On-State Voltage Drop:Transparent Emitter Structure9.6 Current Saturation Model9.6.1 Carrier Distribution:Symmetric Structure9.6.2 Output Characteristics:Symmetric Structure9.6.3 Output Resistance:Symmetric Structure9.6.4 Carrier Distribution:Asymmetric Structure9.6.5 Output Characteristics:Asymmetric Structure9.6.6 Output Resistance:Asymmetric Structure9.6.7 Carrier Distribution:Transparent Emitter Structure9.6.8 Output Characteristics:Transparent Emitter Structure9.6.9 Output Resistance:Transparent Emitter Structure9.7 Switching Characteristics9.7.1 Turn-On Physics:Forward Recovery9.7.2 Turn-Off Physics:No-Load Conditions9.7.3 Turn-Off Physics:Resistive Load9.7.4 Turn-Off Physics:Inductive Load9.7.5 Energy Loss per Cycle9.8 Power Loss

<<功率半导体器件基础>>

Optimization9.8.1 Symmetric Structure9.8.2 Asymmetric Structure9.8.3 Transparent Emitter Structure9.8.4 Comparison of Tradeoff Curves9.9 Complementary(P-Channel)Structure9.9.1 On-State Characteristics9.9.2 Switching Characteristics9.9.3 Power Loss Optimization9.10 Latch-Up Suppression9.10.1 Deep P+ Diffusion9.10.2 Shallow P+ Layer9.10.3 Reduced Gate Oxide Thickness9.10.4 Bipolar Current Bypass9.10.5 Diverter Structure9.10.6 Cell Topology9.10.7 Latch-Up Proof Structure9.11 Safe Operating Area9.11.1 Forward-Biased Safe Operating Area9.11.2 Reverse-Biased Safe Operating Area9.11.3 Short-Circuit Safe Operating Area9.12 Trench-Gate Structure9.12.1 Blocking Mode9.12.2 On-State Carrier Distribution9.12.3 On-State Voltage Drop9.12.4 Switching Characteristics9.12.5 Safe Operating Area9.12.6 Modified Structures9.13 Blocking Voltage Scaling9.13.1 N-Base Design9.13.2 Power MOSFET Baseline9.13.3 On-State Characteristics9.13.4 Tradeoff Curve9.14 High Temperature Operation9.14.1 On-State Characteristics9.14.2 Latch-Up Characteristics9.15 Lifetime Control Techniques9.15.1 Electron Irradiation9.15.2 Neutron Irradiation9.15.3 Helium Irradiation9.16 Cell Optimization9.16.1 Planar-Gate Structure9.16.2 Trench-Gate Structure9.17 Reverse Conducting Structure9.18 SummaryProblemsReferencesChapter 10 Synopsis10.1 Typical H-Bridge Topology10.2 Power Loss Analysis10.3 Low DC Bus Voltage Applications10.4 Medium DC Bus Voltage Applications10.5 High DC Bus Voltage Applications10.6 SummaryProblemsReferencesIndex

<<功率半导体器件基础>>

版权说明

本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问:<http://www.tushu007.com>