

<<系统集成>>

图书基本信息

书名 : <<系统集成>>

13位ISBN编号 : 9787030182555

10位ISBN编号 : 7030182553

出版时间 : 2007-1

出版时间 : 科学

作者 : 霍夫曼

页数 : 490

版权说明 : 本站所提供之下载的PDF图书仅提供预览和简介,请支持正版图书。

更多资源请访问 : <http://www.tushu007.com>

<<系统集成>>

内容概要

本书介绍了涉及集成电路组件的集成和设计的较宽范围的内容，提供给读者用简单公式估计晶体管几何尺寸和推演电路行为的方法。

这本独特的书广泛覆盖场效应管的设计、MOS管的建模和数字CMOS集成电路设计基础以及MOS存储器结构和设计。

本书突出了在片上系统设计和集成方面知识增加的需求，第一次在单本中覆盖半导体物理学、数字VLSI设计和模拟集成电路，介绍了集成电路半导体组件的基本行为和基于MOS与BiCMOS工艺的数字和模拟集成电路的设计。

<<系统集成>>

书籍目录

Preface Acknowledgments Physical Constants and Conversion Factors Symbols 1 Semiconductor Physics 1.1 Band Theory of Solids 1.2 Doped Semiconductor 1.3 Semiconductor in Equilibrium 1.3.1 Fermi-Dirac Distribution Function 1.3.2 Carrier Concentration at Equilibrium 1.3.3 Density Product at Equilibrium 1.3.4 Relationship between Energy, Voltage, and Electrical Field 1.4 Charge Transport 1.4.1 Drift Velocity 1.4.2 Drift Current 1.4.3 Diffusion Current 1.4.4 Continuity Equation 1.5 Non-Equilibrium Conditions Problems References Further Reading 2 pn-Junction 2.1 Inhomogeneously Doped n-type Semiconductor 2.2 pn-Junction at Equilibrium 2.3 Biased pn-Junction 2.3.1 Density Product under Non-Equilibrium Conditions 2.3.2 Current-Voltage Relationship 2.3.3 Deviation from the Current-Voltage Relationship 2.3.4 Voltage Reference Point 2.4 Capacitance Characteristic 2.4.1 Depletion Capacitance 2.4.2 Diffusion Capacitance 2.5 Switching Characteristic 2.6 Junction Breakdown 2.7 Modeling the pn-Junction 2.7.1 Diode Model for CAD Applications 2.7.2 Diode Model for Static Calculations 2.7.3 Diode Model for Small-Signal Calculations Problems References 3 Bipolar Transistor 3.1 Bipolar Technologies 3.2 Transistor Operation 3.2.1 Current-Voltage Relationship 3.2.2 Transistor under Reverse Biased Condition 3.2.3 Voltage Saturation 3.2.4 Temperature Behavior 3.2.5 Breakdown Behavior 3.3 Second-Order Effects 3.3.1 High Current Effects 3.3.2 Base-Width Modulation 3.3.3 Current Crowding 3.4 Alternative Transistor Structures 3.5 Modeling the Bipolar Transistor 3.5.1 Transistor Model for CAD Applications 3.5.2 Transistor Model for Static Calculations 3.5.3 Transistor Model for Small-Signal Calculations 3.5.4 Transit Time Determination Problems References Further Reading 4 MOS Transistor 4.1 CMOS Technology 4.2 The MOS Structure 4.2.1 Characteristic of the MOS Structure 4.2.2 Capacitance Behavior of the MOS Structure 4.2.3 Flat-Band Voltage 4.3 Equations of the MOS Structure 4.3.1 Charge Equations of the MOS Structure 4.3.2 Surface Voltage at Strong Inversion 4.3.3 Threshold Voltage and Body Effect 4.4 MOS Transistor 4.4.1 Current-Voltage Characteristic at Strong Inversion 4.4.2 Improved Transistor Equation 4.4.3 Current-Voltage Characteristic at Weak Inversion 4.4.4 Temperature Behavior 4.5 Second-Order Effects 4.5.1 Mobility Degradation 4.5.2 Channel Length Modulation 4.5.3 Short Channel Effects 4.5.4 Hot Electrons 4.5.5 Gate-Induced Drain Leakage 4.5.6 Breakdown Behavior 4.5.7 Latch-up Effect 4.6 Power Devices 4.7 Modeling of the MOS Transistor 4.7.1 Transistor Model for CAD Applications 4.7.2 Transistor Model for Static and Dynamic Calculations 4.7.3 Transistor Model for Small-Signal Calculations Problems Appendix A Current-Voltage Equation of the MOS Transistor under Weak Inversion Condition References Further Reading 5 Basic Digital CMOS Circuits 5.1 Geometric Design Rules 5.2 Electrical Design Rules 5.3 MOS Inverter 5.3.1 Depletion Load Inverter 5.3.2 Enhancement Load Inverter 5.3.3 PMOS Load Inverter 5.3.4 CMOS Inverter 5.3.5 Ratioed Design Issues 5.4 Switching Performance of the Inverters 5.5 Buffer Stages 5.5.1 Super Buffer 5.5.2 Bootstrap Buffer 5.6 Input/Output Stage 5.6.1 Input Stage 5.6.2 Output Stage 5.6.3 ESD Protection Problems References 6 Combinational and Sequential CMOS Circuits 6.1 Static Combinational Circuits 6.1.1 Complementary Circuits 6.1.2 PMOS Load Circuits 6.1.3 Pass-Transistor Circuits 6.2 Clocked Combinational Circuits 6.2.1 Clocked CMOS Circuits (C2MOS) 6.2.2 Domino Circuits 6.2.3 NORA Circuits 6.2.4 Differential Cascaded Voltage Switch Circuits (DCVS) 6.2.5 Switching Performance of Ratioless Logic 6.3 High Speed Circuits 6.4 Logic Arrays 6.4.1 Decoder 6.4.2 Programmable Logic Array 6.5 Sequential Circuits 6.5.1 Flip-flop 6.5.2 Two-Phase Clocked Register 6.5.3 One-Phase Clocked Register 6.5.4 Clock Distribution and Generation Problems References Further Reading 7 MOS Memories 7.1 Read Only Memory 7.2 Electrically Programmable and Optically Erasable Memory 7.2.1 EPROM Memory Architecture 7.2.2 Current Sense Amplifier 7.3 Electrically Erasable and Programmable Read Only Memories 7.3.1 EEPROM Memory Cells 7.3.2 Flash Memory Architectures 7.3.3 On-Chip Voltage Generators 7.4 Static Memories 7.4.1 Static Memory Cells 7.4.2 SRAM Memory Architecture 7.4.3 Address Transition Detection 7.5 Dynamic Memories 7.5.1 One-Transistor Cell 7.5.2 Basic DRAM Memory Circuits 7.5.3 DRAM Architecture 7.5.4 Radiation Effects in Memories Problems References Further Reading 8 Basic Analog CMOS Circuits 8.1 Current Mirror 8.1.1 Improved Current Sources 8.2 Source Follower 8.3 Basic Amplifier Performance 8.3.1 Miller Effect 8.3.2 Differential Stage with Symmetrical Output 8.3.3 Differential Input Stage with Single-Ended Output Problems Appendix A Transfer

<<系统集成>>

Functions
Further Reading
9 CMOS Amplifiers
9.1 Miller Amplifier
9.2 Folded Cascode Amplifier
9.3 Folded Cascode Amplifier with Improved Driving Capability
Problems
References
10 BICMOS
10.1 Current Steering Techniques
10.1.1 CML Circuits
10.1.2 ECL Circuits
10.2 BICMOS Buffer and Gates
10.3 Band-Gap Reference Circuits
10.4 Analog Applications
10.4.1 Offset Voltage of Bipolar and MOS Transistors
10.4.2 Comparison of Small-Signal Performance
Problems
References
Index

<<系统集成>>

编辑推荐

本书涉及集成电路组件的集成和设计的较宽范围的内容，提供给读者用简单公式估计晶体管几何尺寸和推演电路行为的方法。

本书广泛覆盖场效应管的设计、MOS管的建模和数字CMOS集成电路设计基础以及MOS存储器结构和设计。

本书突出了片上系统设计和集成方面知识的需求，在单本书中覆盖半导体物理学、数字VLSI设计和模拟集成电路，介绍了集成电路半导体组件的基本行为和基于CMOS与BiCMOS工艺的数字和模拟集成电路的设计。

<<系统集成>>

版权说明

本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问:<http://www.tushu007.com>